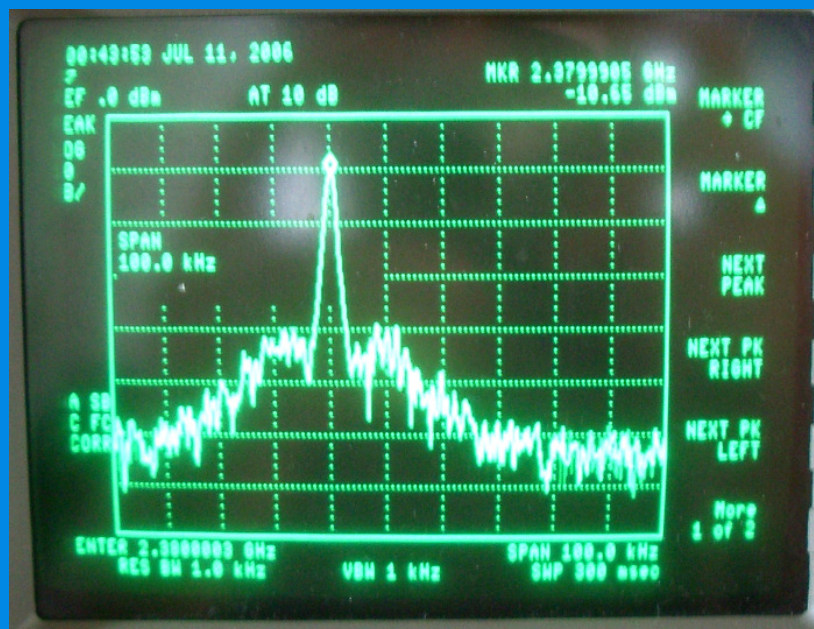


HSSDT

High Speed Satellite Data Transmitter



From 400 to 6100 Mhz FFSK Modulator based on N-Fractional PLL

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Introduction

This presentation describes the project: **HSSDT** – “*High Speed Satellite Data Transmitter*” a data-transmitter for *on-board Microsatellite use*, composed by a Microchip microcontroller **PIC16F628** driving an N-fractional synthesizer:

SKY72302 *from Skyworks*

This project can guarantee an high speed data link following, however, the low-cost requirements.

The configuration is capable to generate an FFSK Direct Digital Modulation (DDM) in the PLL range (400 – 6100 Mhz) This system work at the data rate of 38.4kbps and, can reach a speed over 153kbps.

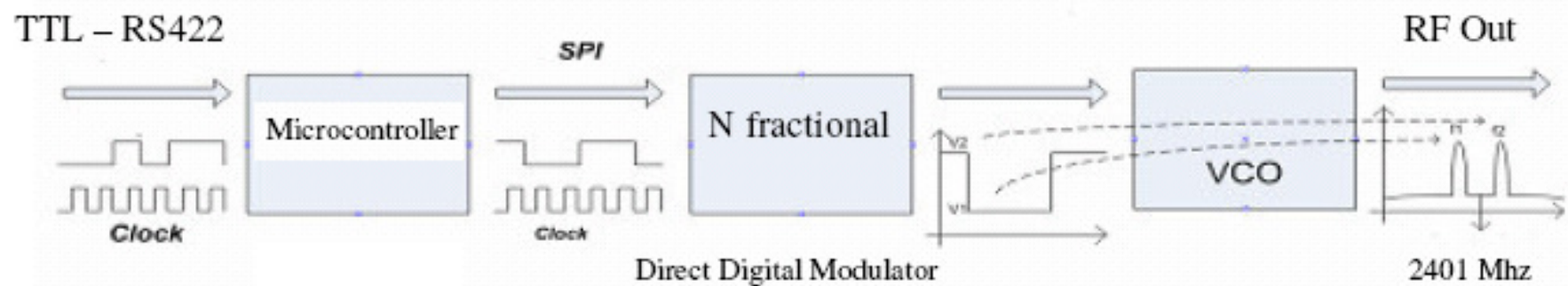
This work represent my last collaboration, as RF-Engineer, inside the team ALMASat, Microsatellite of the University of Bologna (ITALY) [ref. **ALMASat Microsatellite-Platform for Small Scientific Experiments – Giulio Pezzi AB2VY** - 2007 AMSAT-North America Space Symposium and Annual Meeting October 26-28, 2007 Pittsburgh PA]

Another version of this project, using ATMEL Microcontroller ATMega32 instead of Microchip PIC, is present on the proceeding papers of this year

Outline of HSSDT Project

- Link Design
 - > Background on FFSK modulation
 - Direct Digital Modulation technique (DDM)
 - Example of Satellite Link Budget
- Ground Station Overview
 - > Receiving Systems
- S-Band Telemetry Transmitter for Microsatellite
 - > Top-level configuration and PA design
 - > N-Synthesizer CX72302
 - > A very simple design using **Microchip PIC16F628 μ controller**
 - > Microcontroller and power supply control
- Possible improvements and conclusions

S-band Link Design



Design Approach

- The proposed design is based on the following key points:
 - *Use of COTS by Yaesu-Icom-Kenwood and classic 38k4Bd Tnc equipment for Ground Station assembling;*
 - *Use of Direct Modulation techniques for generating high-rate S-Band down-link.*

Just a reminder on modulation technique....

- The selected modulation scheme is the Fast Frequency-Shift Keying (FFSK).
- The FFSK corresponds to a Continuous Phase Frequency-Shift Keying (CPFSK) in which the modulation index h has been selected equal to 0.5, i.e.:

$$h = \Delta f \cdot T = 0.5$$

being T the symbol period and Δf the peak-to-peak frequency deviation.

- The FFSK power spectral density $G(f)$ is given by:

$$G(f) = \frac{8P_c T}{\pi^2} \cdot \frac{1 + \cos(4\pi f T)}{(1 - 16f^2 T^2)^2}$$

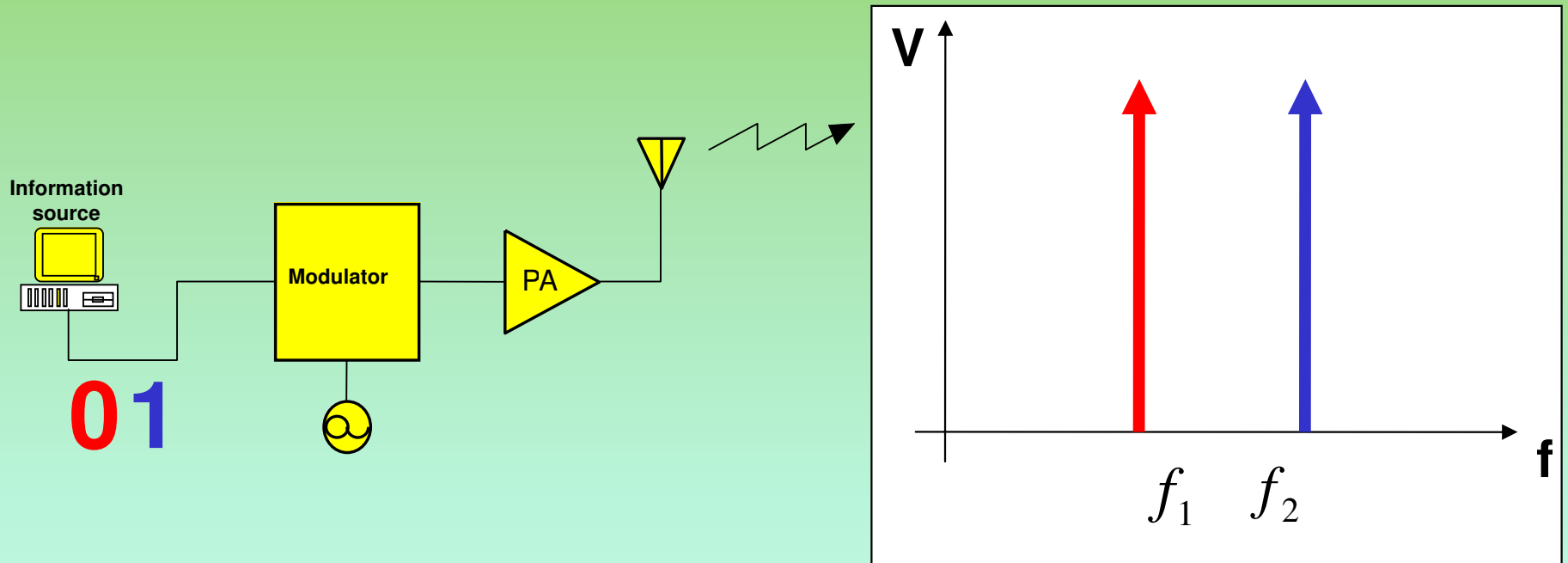
where P_c is the signal power.

- The main lobe contains the 99.5% of the power and spectral nulls are at $\pm 0.75/T$ from the carrier.

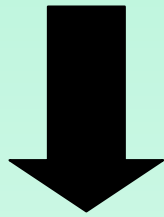
Why we use an N-fractional Modulator (SKY72302) ?

- A combination of a large bandwidth, fine resolution, and the three-wire high-speed serial interface allows for a direct frequency modulation of the VCO.
- This supports any *continuous phase constant envelope modulation* scheme such as :
 - Frequency Modulation (FM),
 - Frequency Shift Keying (FSK)
 - Minimum Shift Keying (MSK)
 - Gaussian Minimum Shift Keying (GMSK)

Direct Digital Modulation (DDM)

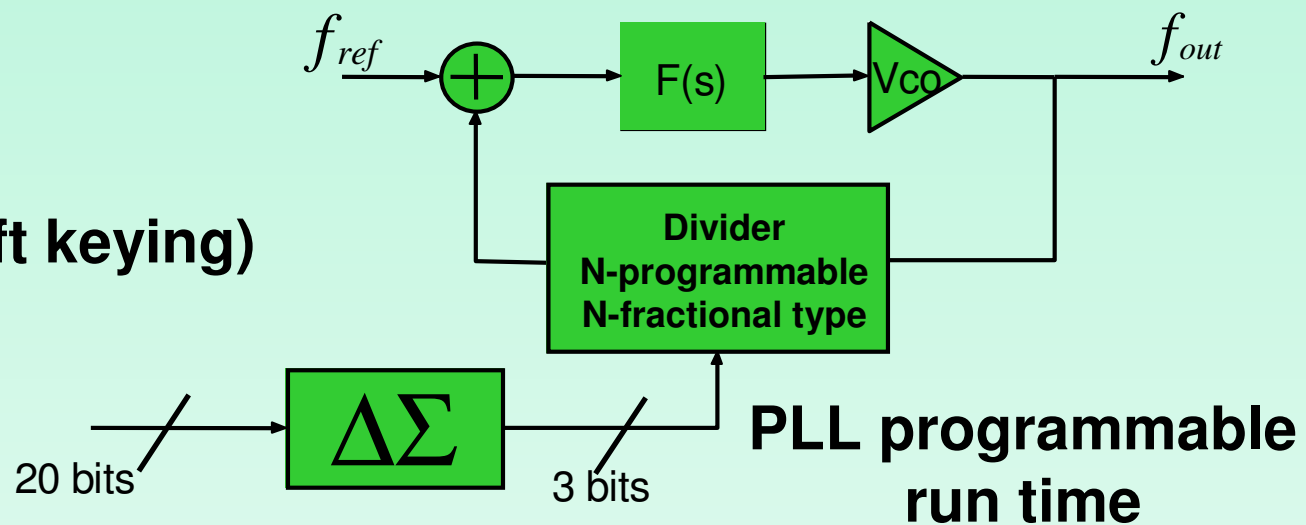


DDM



FSK (Frequency shift keying)

0 → f_1
1 → f_2



Link budget @ 38.4 Kbps with 2 Watts PA

Item	Parameter	Unit	Worst Case	Best Case	Note
1	Bit Rate	[bps]	38400,0	38400,0	Signal BW = 1.5 x (Bit Rate) for FFSK With 2 W PA prototype EIRP Worst = 7.1 W , Best = 7.5 W
2	Signal Bandwidth	[Hz]	57600,0	57600,0	
3	Tx Frequency	[MHz]	2401,0	2401,0	
4	Tx Ouput Power	[W]	2,0	2,0	
5	Tx Ouput Power	[dBW]	3,0	3,0	
6	Circuit Loss	[dB]	-0,5	-0,2	
7	Tx Antenna Gain	[dBi]	6,0	6,0	
8	EIRP	[dBW]	8,5	8,8	
9	Path Length	[km]	3300,0	650,0	
10	Free-Space Loss	[dB]	-170,4	-156,3	
11	Ionosperic-Tropospheric Loss	[dB]	-0,5	-0,5	
12	Pointing Loss	[dB]	-2,0	-0,2	Preliminary value was 17.8 dBi
13	Polarization Loss	[dB]	-1,0	-0,2	
14	Rx Antenna Gain	[dBi]	22,0	22,0	
15	Received Power	[dBW]	-143,4	-126,4	
16	Received Power	[dBm]	-113,4	-96,4	
17	Boltzmann's Constant	[W/K Hz]	1,38E-23	1,38E-23	Including sky and ground contribution (elevation angle > 30°)
18	Boltzmann's Constant	[dBW/K Hz]	-228,6	-228,6	
19	Antenna Noise Temperature	[K]	50,0	50,0	
20	Receiver Noise Figure	[dB]	4,5	4,5	
21	Receiver Noise Temperature	[K]	527,3	527,3	
22	System Noise Temperature	[K]	577,3	577,3	
23	Equivalent Noise Density	[dBW/Hz]	-201,0	-201,0	
24	Equivalent Noise Density	[dBm/Hz]	-171,0	-171,0	
25	C/No	[dBHz]	57,6	74,6	Eb/No required for a BER of 10 ⁻⁵
26	Eb/No	[dB]	11,7	28,7	
27	Threshold Eb/No	[dB]	13,4	13,4	
28	Link Margin	[dB]	-1,6	15,4	

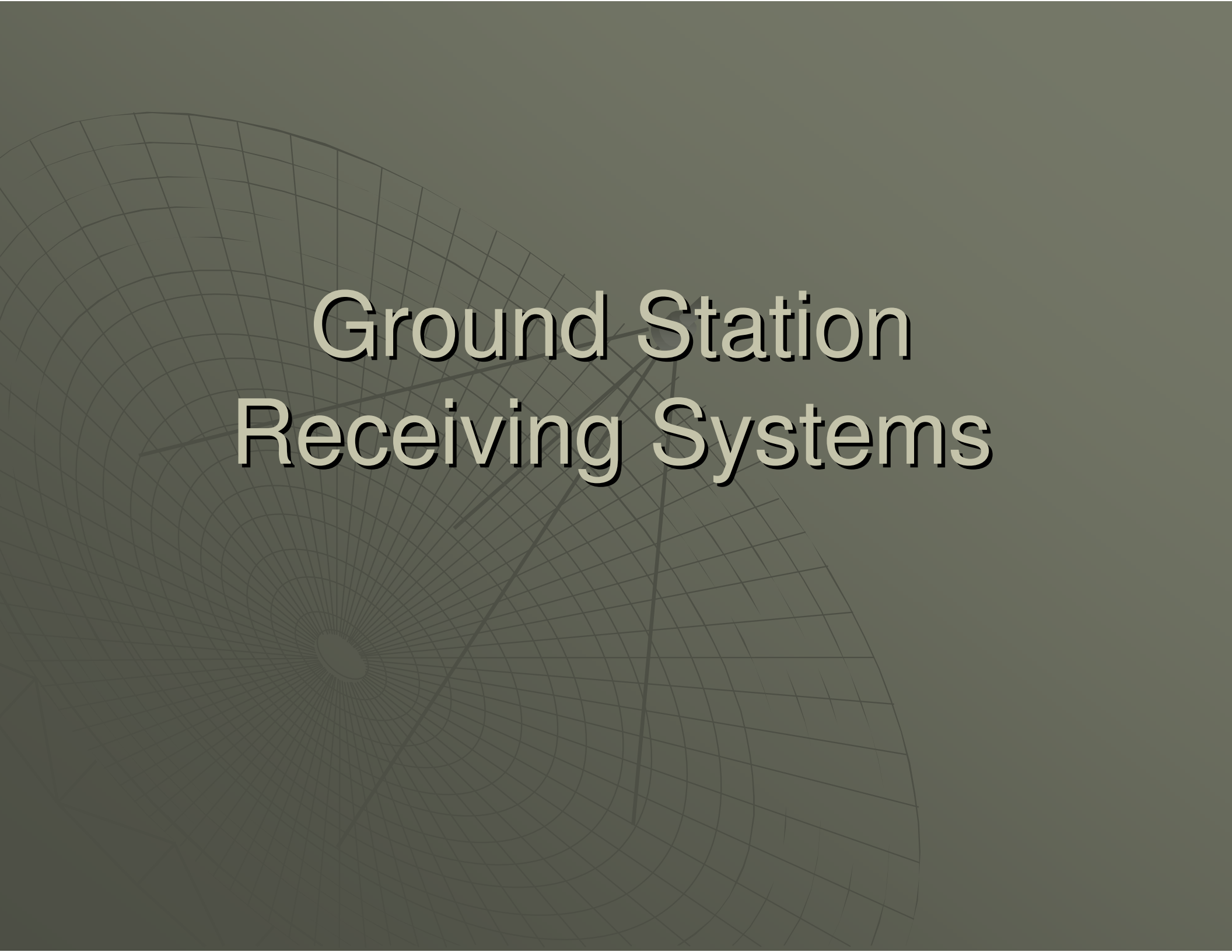
Link budget @ 153.6 Kbps with 8 Watts PA

Item	Parameter	Unit	Worst Case	Best Case	Note
1	Bit Rate	[bps]	153600,0	153600,0	Signal BW = 1.5 x (Bit Rate) for FFSK With 8 W PA prototipe see next slides... EIRP Worst = 28.2 W , Best = 30.2 W
2	Signal Bandwidth	[Hz]	230400,0	230400,0	
3	Tx Frequency	[MHz]	2401,0	2401,0	
4	Tx Ouput Power	[W]	8,0	8,0	
5	Tx Ouput Power	[dBW]	9,0	9,0	
6	Circuit Loss	[dB]	-0,5	-0,2	
7	Tx Antenna Gain	[dBi]	6,0	6,0	
8	EIRP	[dBW]	14,5	14,8	
9	Path Length	[km]	3300,0	650,0	
10	Free-Space Loss	[dB]	-170,4	-156,3	
11	Ionosperic-Tropospheric Loss	[dB]	-0,5	-0,5	
12	Pointing Loss	[dB]	-2,0	-0,2	Preliminary value was 17.8 dBi
13	Polarization Loss	[dB]	-1,0	-0,2	
14	Rx Antenna Gain	[dBi]	22,0	22,0	
15	Received Power	[dBW]	-137,4	-120,4	
16	Received Power	[dBm]	-107,4	-90,4	
17	Boltzmann's Constant	[W/K Hz]	1,38E-23	1,38E-23	Including sky and ground contribution (elevation angle > 30°)
18	Boltzmann's Constant	[dBW/K Hz]	-228,6	-228,6	
19	Antenna Noise Temperature	[K]	50,0	50,0	
20	Receiver Noise Figure	[dB]	4,5	4,5	
21	Receiver Noise Temperature	[K]	527,3	527,3	
22	System Noise Temperature	[K]	577,3	577,3	
23	Equivalent Noise Density	[dBW/Hz]	-201,0	-201,0	
24	Equivalent Noise Density	[dBm/Hz]	-171,0	-171,0	
25	C/No	[dBHz]	63,6	80,6	Eb/No required for a BER of 10 ⁻⁵
26	Eb/No	[dB]	11,7	28,7	
27	Threshold Eb/No	[dB]	13,4	13,4	
28	Link Margin	[dB]	-1,6	15,4	

Possible speeds for data-transfers

The following speeds are possible but, in our case, we are limited to 153.6 kbps for the internal main board clock (20 Mhz) that we will see in the next slides..

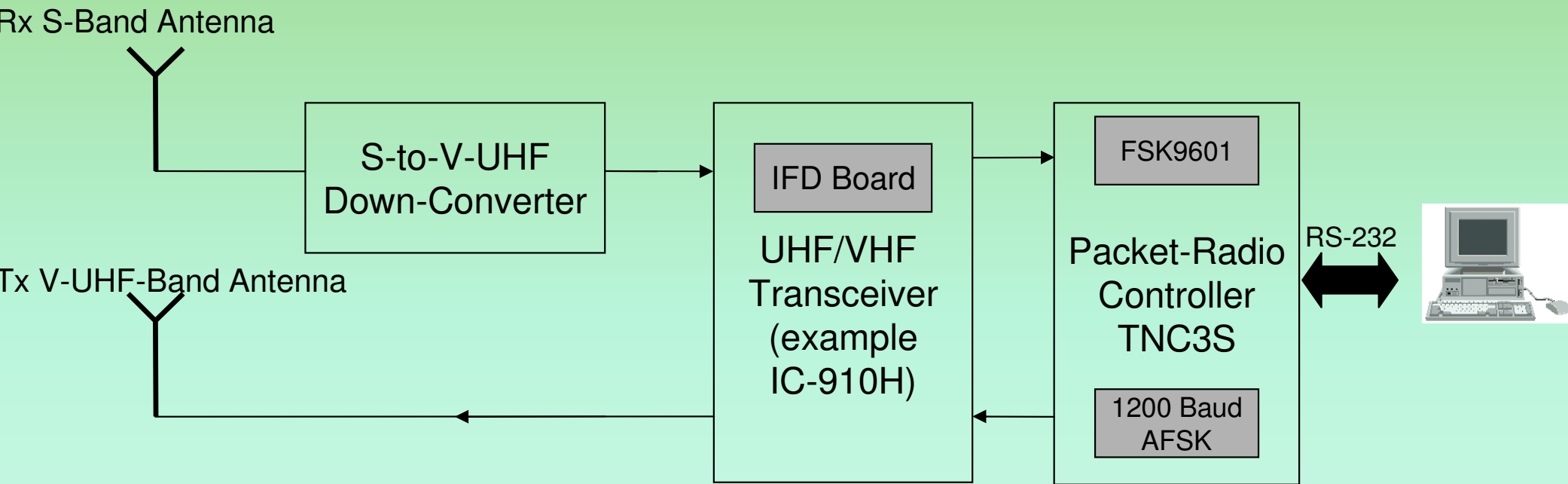
- 4.8 Kbps
- 9.6 Kbps
- 19.2 Kbps
- 38.4 Kbps  With 20 Mhz clock speed on μ Pc board
- 76.8 Kbps
- 153.6 Kbps
- 307.2 Kbps
- 614.4 Kbps  With higher clock speed (> 20 Mhz) on μ Pc board
- 1.228 Mbps



Ground Station Receiving Systems

On-Ground Station: Block Diagram

- Block Diagram

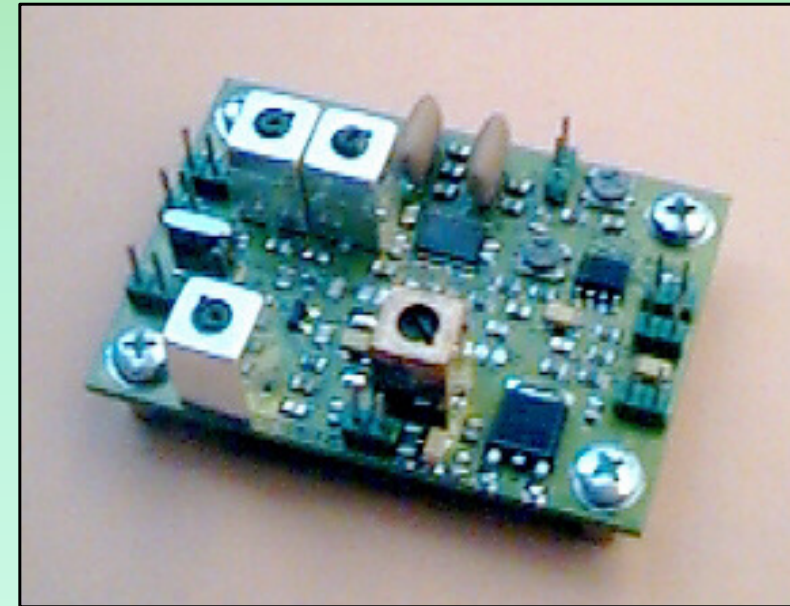


- The TNC3S houses two modems:**

- 1200 Baud AFSK (i.e. Bell 202) for up-link commanding
- FSK9601 (i.e. G3RUH) proper enhanced to achieve 19200/38400 bps as requested by the down-link telemetry.

On-Ground Station: Hardware Description

- The **IFD board** provided by SYMEK can be used to expand the capabilities of the Icom IC-910H to high speed data reception as 38400, 76800 and up to 153600 bps.
- The IF signal of the ICOM IC-910H is tapped directly behind the RF front-end and connected to the input of the IFD module, performing a frequency conversion down to IF by a mixer circuit and a fixed frequency crystal oscillator.

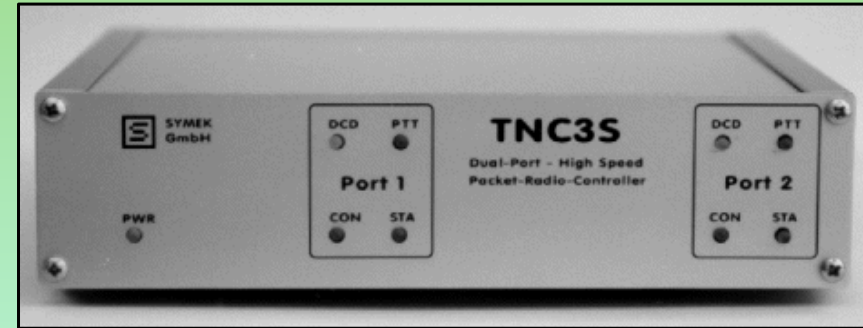


IFD Board

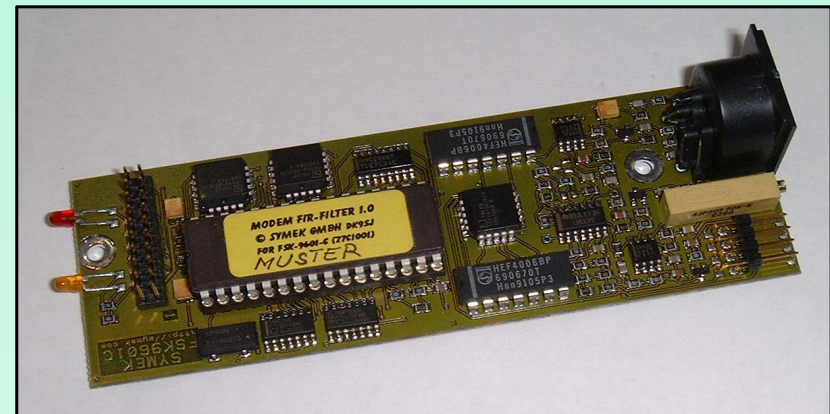
- The bandwidth of the IFD amplifier is designed to match the required data rate. For the considered applications (i.e. 38400 bps) the IFD bandwidth is equal to 80 kHz.

On-Ground Station: Hardware Description

- The Packed-Radio-Controller **TNC3S** (by Symek) includes the **FSK9601 Modem** to convert the audio-signals of the radio into digital information and transfer them to the computer and vice-versa. The TNC is connected to the PC via a serial RS232-cable to the COM-interface.
- The FSK9601 Modem is designed for 9600 bps and it can be modified to other data rates in the range from 4800 bps up to 614 kbps by changing some components and jumpers.
 - The baseband filters are customisable properly programming the FSK9601 EPROM;
 - The FSK9601 shall route NRZ symbol at the TNC.



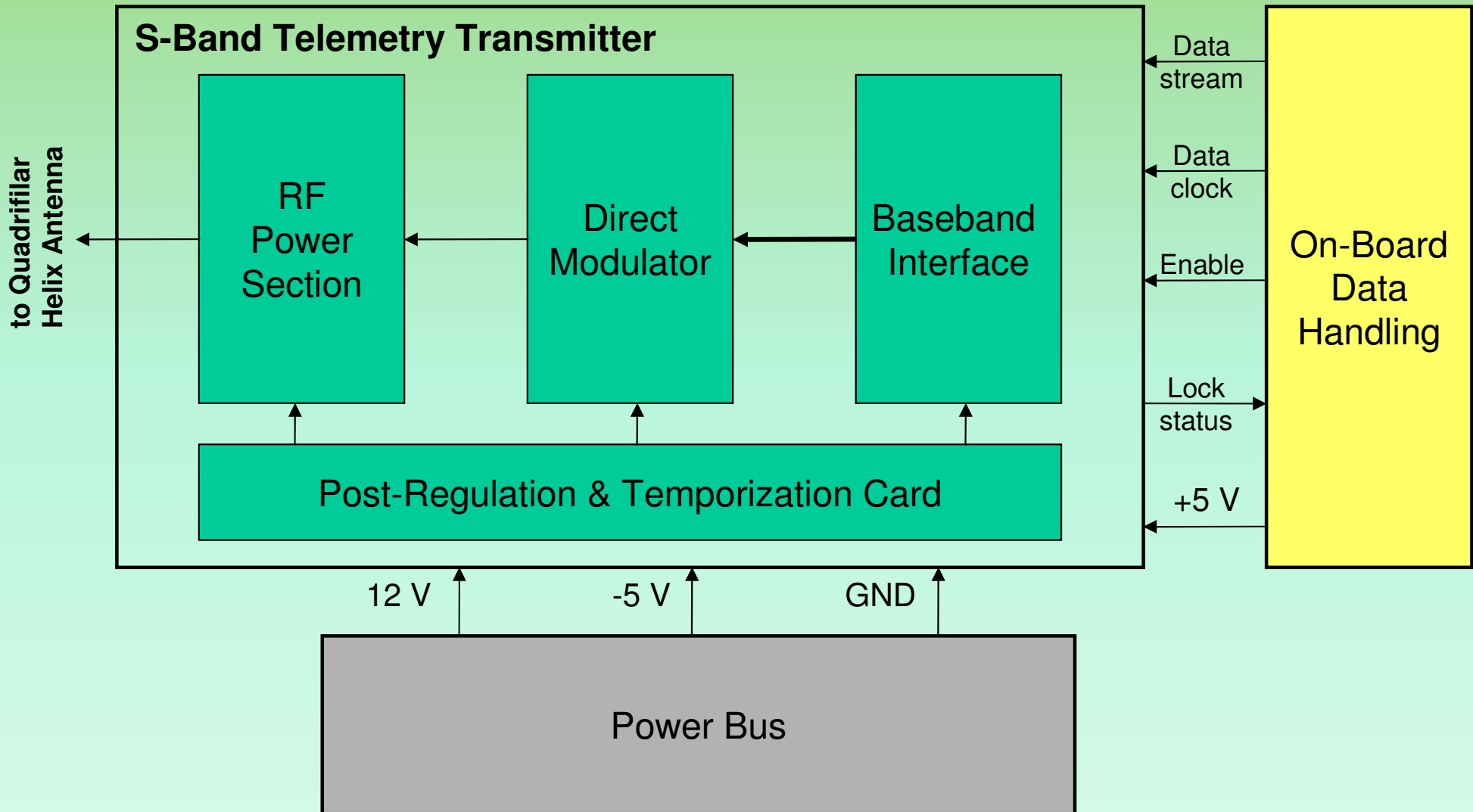
Symek TNC3S



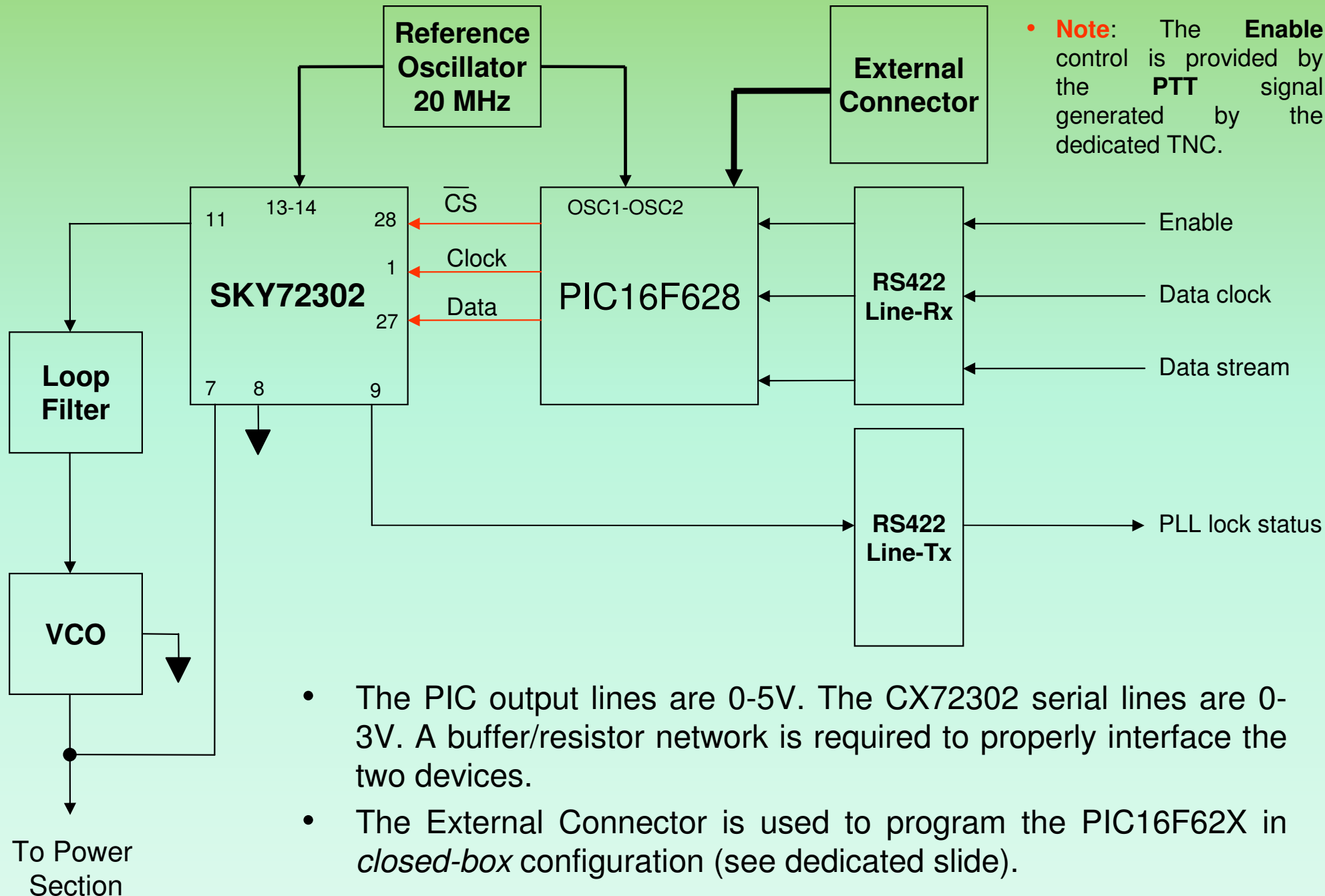
FSK9601 Modem Board

S-Band Telemetry Transmitter for Microsatellite

S-Band Telemetry Sub-system example: Overview



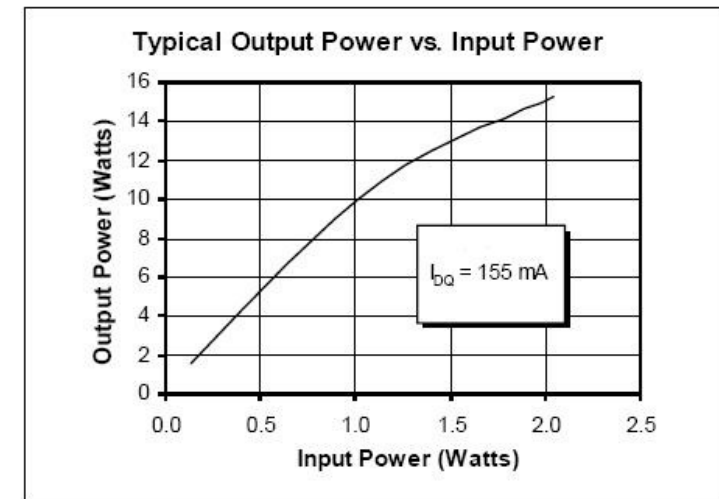
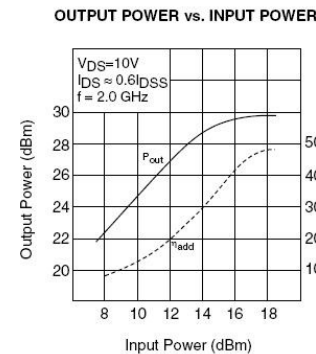
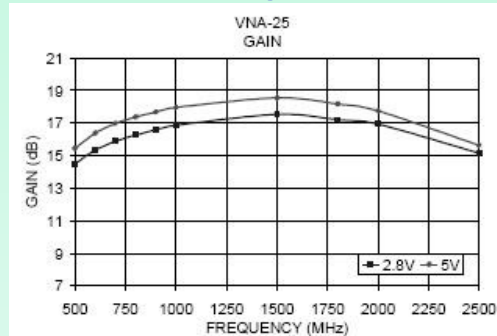
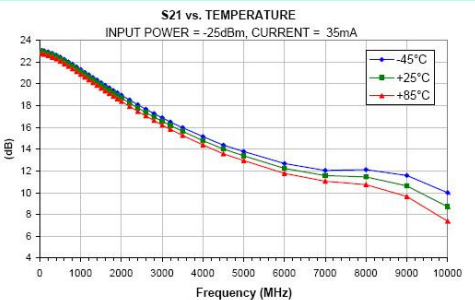
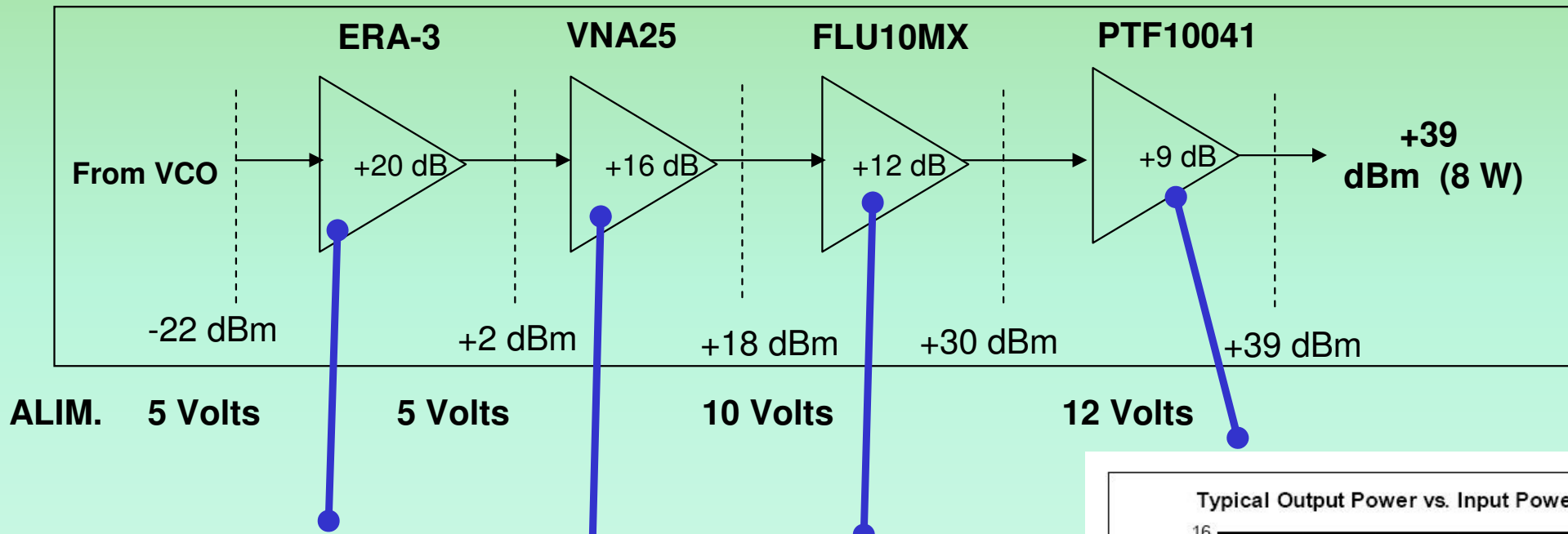
S-Band Telemetry Transmitter: Detailed Design



- The PIC output lines are 0-5V. The CX72302 serial lines are 0-3V. A buffer/resistor network is required to properly interface the two devices.
- The External Connector is used to program the PIC16F62X in *closed-box* configuration (see dedicated slide).

S-Band Telemetry Transmitter: PA Design

- The Power Amplification section receives **-22 dBm** from the S-Band VCO and it shall deliver **+39 dBm** to the antenna sub-system.
- As preliminary, the following line-up based on **4 stages chain (57 dB Gain)**



PIC16F628 Overview

- The PIC16F628 are 18-pin, CMOS, FLASH-based 8-bit microcontroller.
- The PIC16F628 uses a **Harvard architecture**, in which, program and data are accessed from separate memories using separate buses.

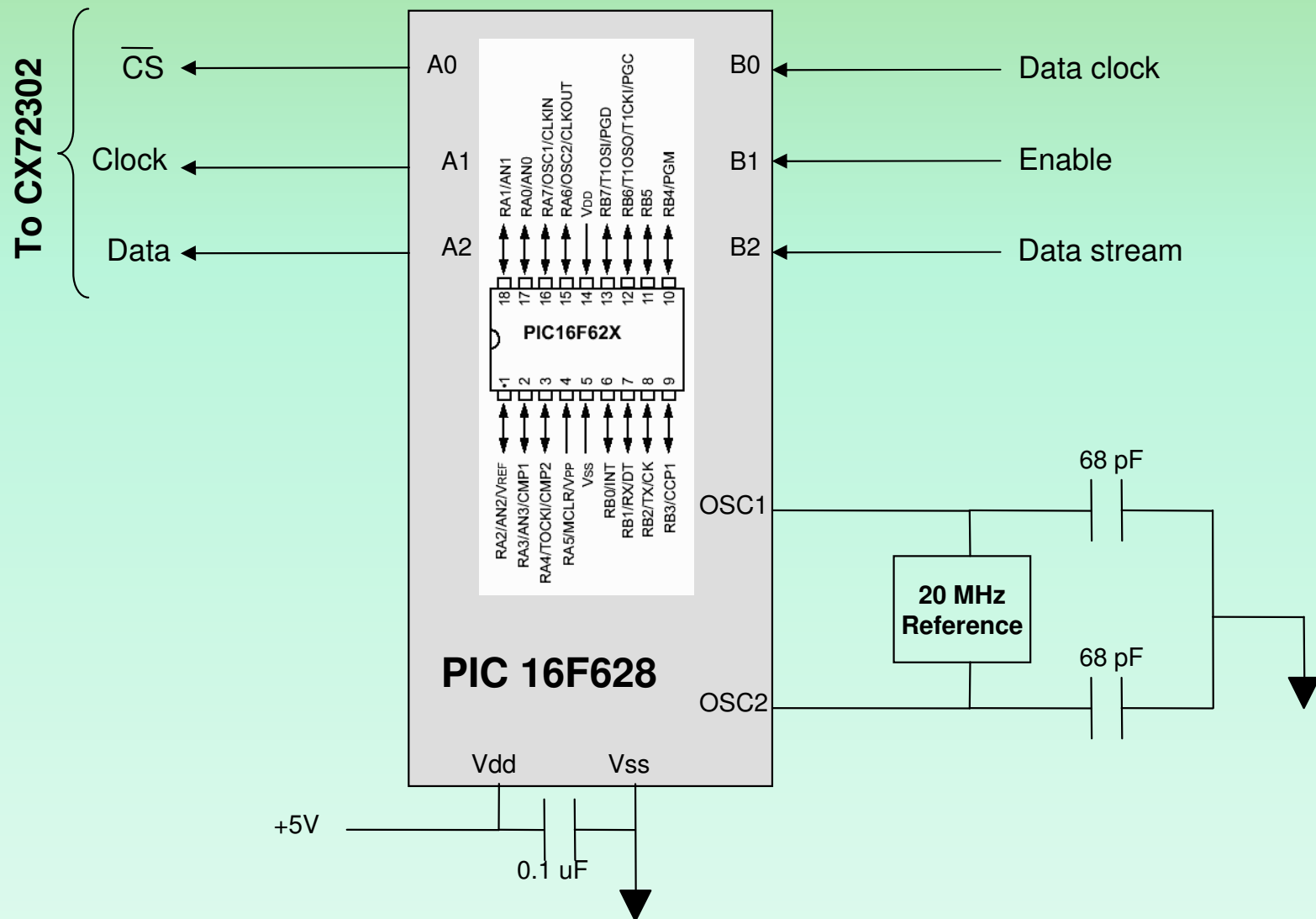
		PIC16F627	PIC16F628	PIC16LF627	PIC16LF628
Clock	Maximum Frequency of Operation (MHz)	20	20	4	4
Memory	FLASH Program Memory (words)	1024	2048	1024	2048
	RAM Data Memory (bytes)	224	224	224	224
	EEPROM Data Memory (bytes)	128	128	128	128
Peripherals	Timer Module(s)	TMR0, TMR1, TMR2	TMR0, TMR1, TMR2	TMR0, TMR1, TMR2	TMR0, TMR1, TMR2
	Comparator(s)	2	2	2	2
	Capture/Compare/PWM modules	1	1	1	1
	Serial Communications	USART	USART	USART	USART
	Internal Voltage Reference	Yes	Yes	Yes	Yes
Features	Interrupt Sources	10	10	10	10
	I/O Pins	16	16	16	16
	Voltage Range (Volts)	3.0-5.5	3.0-5.5	2.0-5.5	2.0-5.5
	Brown-out Detect	Yes	Yes	Yes	Yes
	Packages	18-pin DIP, SOIC, 20-pin SSOP	18-pin DIP, SOIC, 20-pin SSOP	18-pin DIP, SOIC, 20-pin SSOP	18-pin DIP, SOIC, 20-pin SSOP

All PICmicro® Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability. All PIC16F62X Family devices use serial programming with clock pin RB6 and data pin RB7.

Refer to www.microchip.com

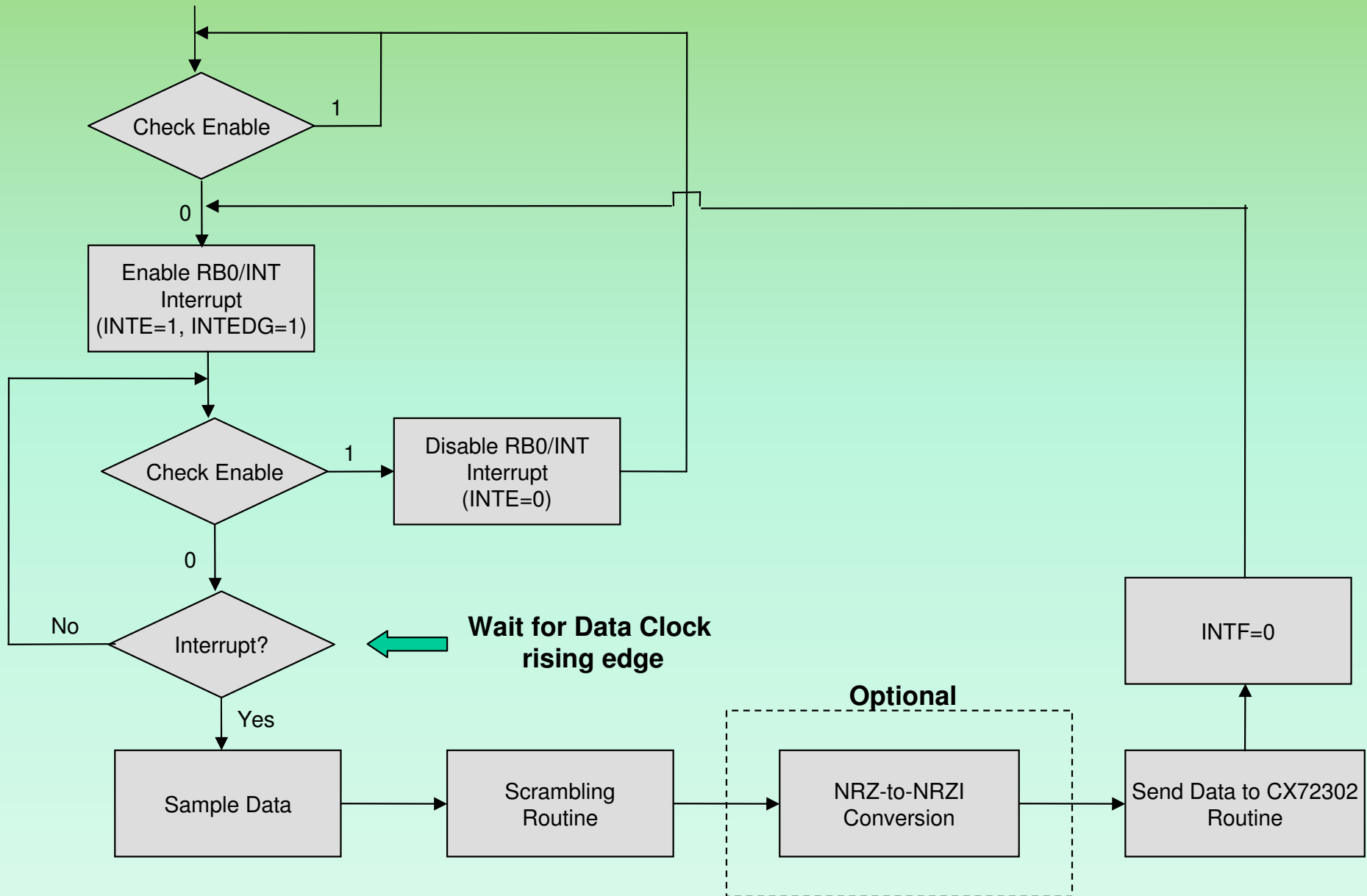
Configuration of PIC16F628

- The PIC16F628 is used as interface between the OBDH sub-system and the CX72302 device.
- The PIC16F628 shall operate in HS mode (using the external 20 MHz reference).



Direct-Modulation SW: Top-Level Flowchart

From Start-Up Configuration routine



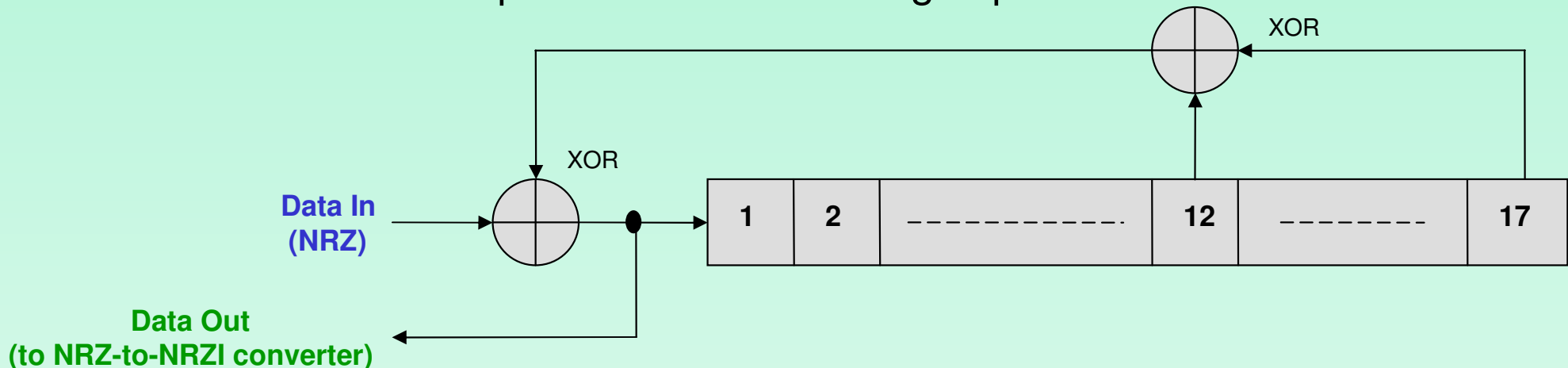
DD-M SW: Just a reminder on G3RUH Scrambling..

- Scrambling is necessary to ensure the required transition density for on-ground receiver bit acquisition and tracking.
- Scrambling is accomplished using part of the 16F628 RAM Data Memory (224 bytes in total) as Linear Feedback Shift register.
- *Scrambling shall be performed according to the G3RUH standard using the following polynomial generator:*

$$f(X)=1+X^{12}+X^{17}$$

where the addition has to be intended modulo-2 (i.e. XOR).

- The above relationship leads to the following implementation:



- The Scrambling memory shall be reset when Enable goes HIGH.

Programming for S-band @ 19.2 kbps

- **Specification:**

- Carrier frequency: $F_{vco_main} = 2401 \text{ MHz}$
- Reference frequency: $F_{ref_main} = 20 \text{ MHz}$
- FFSK modulation: Data Rate = 19.2 kbps → Frequency Deviation = $\pm 14.4 \text{ kHz}$

- **Main Synthesizer Registers Programming:**

$F_{div_ref} = 5 \text{ MHz}$

$F_{div_ref} = F_{vco_main} / (4 \times N_{fractional}) \rightarrow N_{fractional} = 120.05$

$N_{reg} = \text{ROUND}(N_{fractional}) - 32 = 88$

$\text{Dividend} = \text{ROUND}[2^{18} \times (N_{fractional} - N_{reg} - 32)] = 13107$

- **Modulation Control Registers Programming:**

$\text{Step Size} = (20 \text{ MHz} / 4) / 2^{18} \approx 19.07 \text{ Hz}$

$\text{Number of Steps} = \pm 14.4 \text{ kHz} / \text{Step Size} \approx \pm 755 \rightarrow 11 \text{ bit}$

- Using a Magnitude Offset = 6 allows to reduce the modulation data dynamic to 5 bit obtaining a peak frequency deviation of $12 \times 2^6 \times \text{Step Size} = 14.65 \text{ kHz}$ (relative error < 2% w.r.t 14.4 kHz).

- **Verification of Design Constraints:**

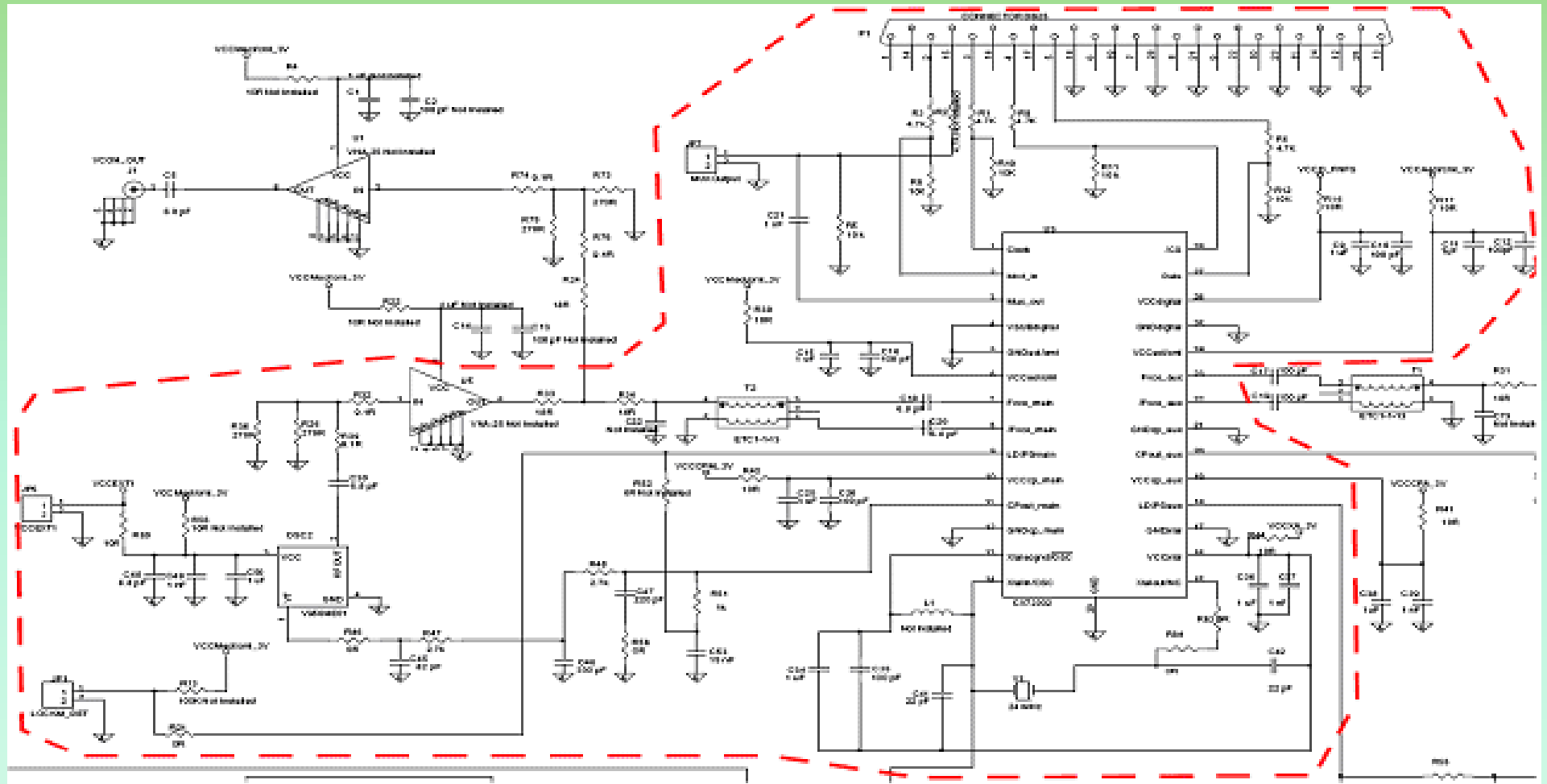
- Maximum data rate:

$$\text{Data Rate}_{\max} = (1/1.5) \times (20 \text{ MHz} / 4) / 100 = 33.3 \text{ kbps}$$

- Minimum serial clock for CX72302 registers programming:

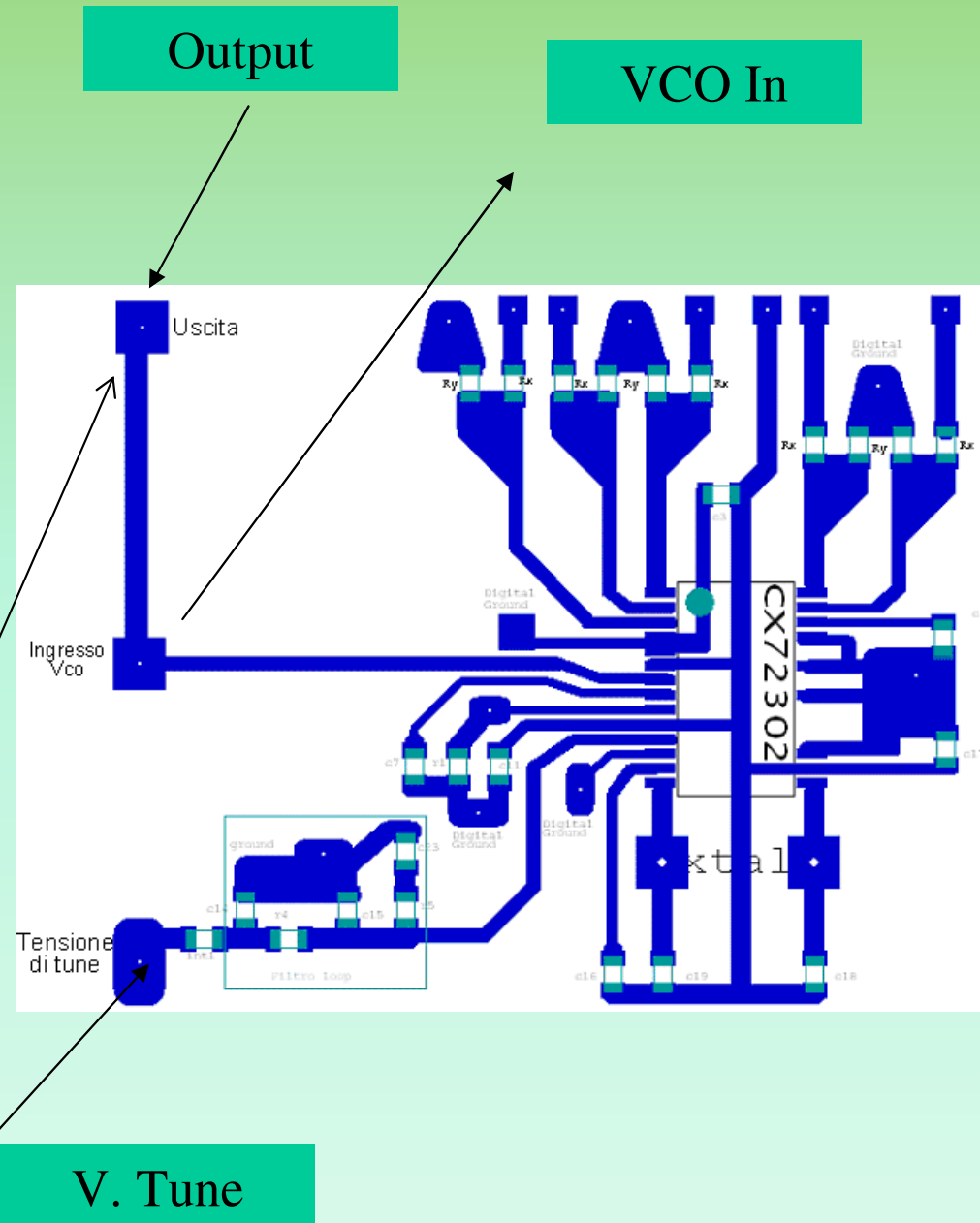
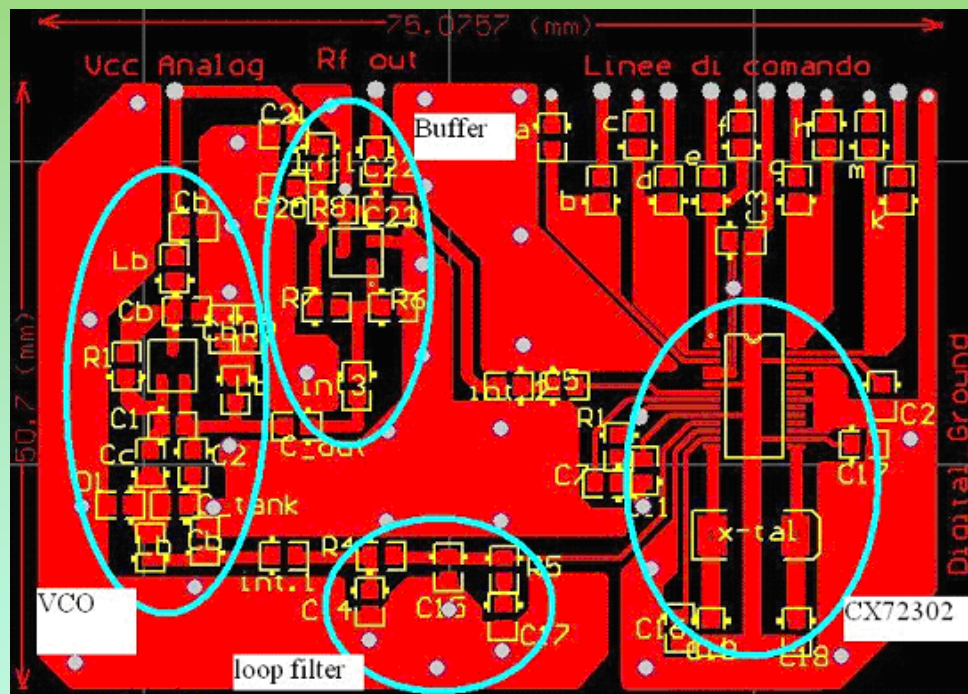
$$\text{Serial Rate}_{\min} = (\text{Data Rate}) \times (\text{Bit per Data}) / (1 - t_3 \times \text{Data Rate}) = 97 \text{ kHz}$$

CX72302 modulator schematics



Schematics parts related to the main synthesizer, used for this application, are shown and highlighted

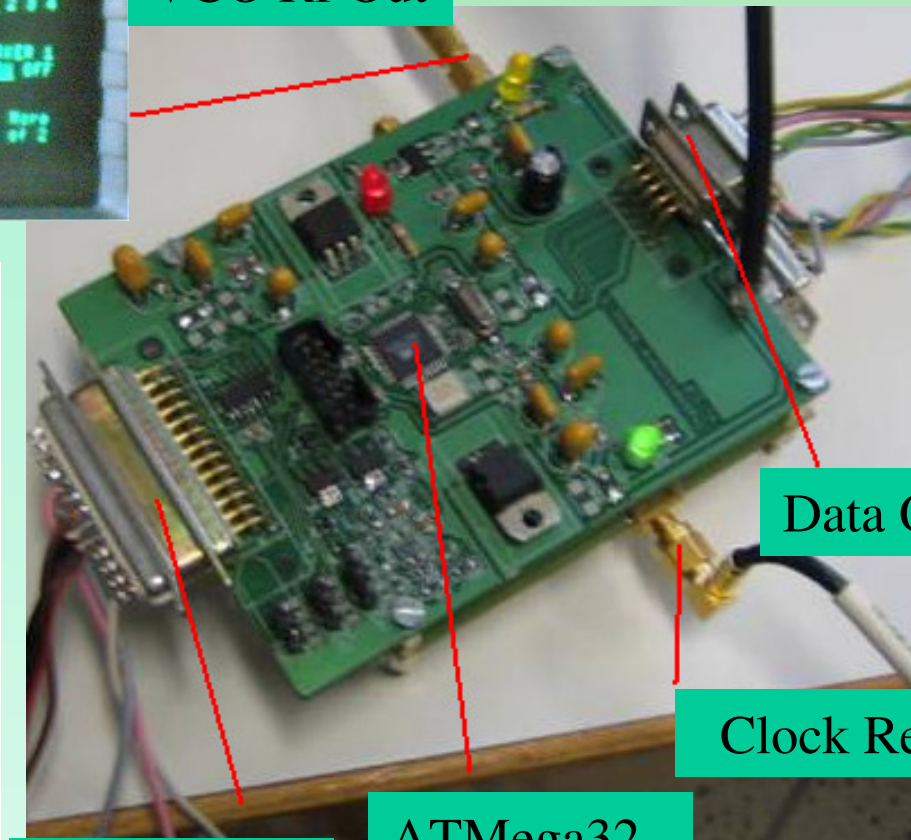
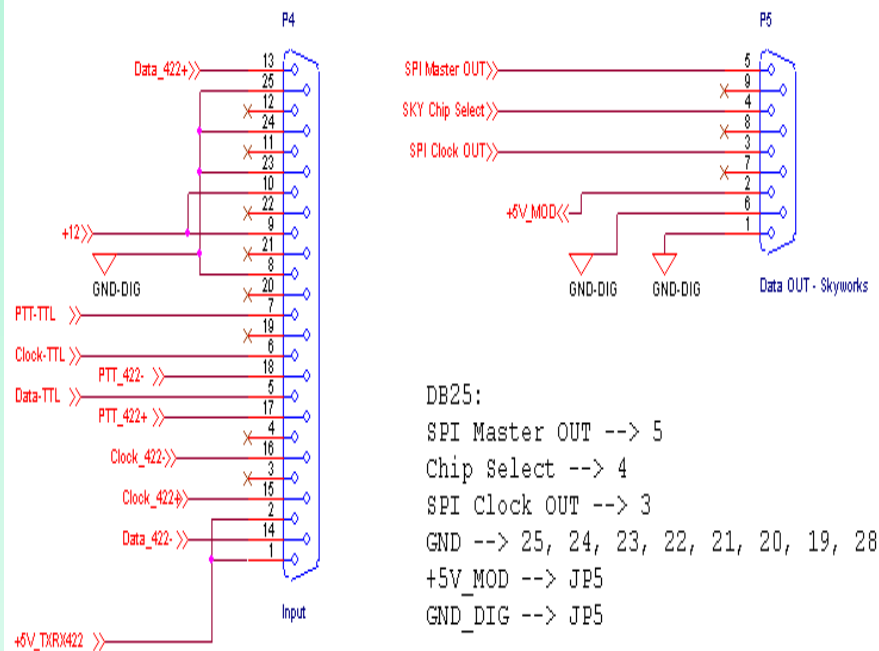
Prototype of CX72302 FSK modulator with integrated VCO



Test of CX72302 FSK modulator with ATmega32 controller



VCO Rf Out



Data Out

Clock Ref.

ATMega32

Data In

Some reasons to replace PIC with AVR.....

1. AVR has non-banked access to data memory, whereas PICs seem to require setting bank registers to access beyond 256 bytes of memory
2. AVR has 32 general purpose registers, the PIC only has one.
3. In AVR that have SRAM (most of them), the stack is contained within SRAM instead of being limited to a built-in hardware stack.
Conversely, with PIC, this is one less thing to worry about.
4. The ATmega have hardware multipliers, PIC16F do not.
5. The AVR appears to support a more generalized interrupt system, as opposed to the PIC high/low priority interrupt vectors.
6. With PIC16F, the memory size is given in 14-bit words, whereas the AVR lists their program sizes in bytes, so the PIC16F's program size capacity is larger than just the number of K would indicate.
7. AVR appears to be a GCC target....

Possible improvements and conclusions

- Increment in performance basically at zero cost
- Configure the modulator “on the fly” to correct frequency deviation due to doppler effect or thermal drift using the fine step of the synthesizer
- Implement an automatic compensation system of oscillators thermal drift
- Changing the VCO it would be possible to set any desired central frequency (400 - 6100 Mhz)

The End ...

73 from ..

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